K means accelerator

# Introduction

## The K means algorithm

The K means algorithm is an iterative algorithm which divides a given data vector to K different clusters (K is a natural number). Each cluster will be characterized by its “center of mass”, what will be referred in this paper as centroid.

### The algorithm steps

For a simpler explanation, it can be assumed that K is a constant predefined natural value. First, some symbols need o be defined:

-the cluster number "*i*" centroid

– the group of points in cluster number "*i*"

Upper index “*t*” – iteration or time

#### Initialization step

The first step in the algorithm is to randomly choose centroids for the K clusters. The “time” (“*t*”) for the initialization step will be defined as zero.

#### Classification step

In each iteration(time) of the algorithm, first each point of the input data is assigned to a cluster based on the “distance” from the point to the clusters centroid. A point will be assigned to cluster number “i” if the metrical distance between it and the cluster’s centroid is the minimum between the distances from the point to all others cluster’s centroids. To simplify:

\*In case of the distance from two different clusters is the same and is the minimum found, the chosen cluster is the one with the lowest index.

#### Centroids update step

After the classification step, the centroids of each cluster are updated to be mean of all points which belong to it in end of iteration(time) *t*. This is done by verifying if a cluster is empty(in this case the centroid is not changed) and then calculating the mean of all the clusters points:

#### Convergence check step

If the centroids of the next iteration calculated in the step above are all equal to the current centroids, then the algorithm comes to an end. Else, the iteration number(time) is increased by one and a new iteration begins with the assigning step.

##### Algorithm convergence

The k means algorithm assures convergence to a local minimum, i.e. the final centroids values are so that the variance within the clusters is minimized while the intra cluster’s variance is maximized. This minimum variance within the cluster is not always the global minimum that can be reached, the local minimum which was reached by the algorithm depends on the initialization step, specifically on the first values of the centroids.

#### Choosing K

Usually the optimal K is not known before the beginning of the algorithm. Therefore, a an error parameter can be defined to help choosing K. The most commonly known error parameter is the clustering error which is defined by:

In this formula, the elements are:

As K increases, the error decreases. For example, if K is as the number of pints in the input vector, the error will be zero. This because it cluster will have just one point which will also be its centroid, but in this case no new information was added by the algorithm.

One suggested method of choosing a natural K so the clustering error is minimized is by gradually increasing K and calculating for each increasement. The process ends when the error reaches a value so that , where is a predefined threshold.

## AMBA APB

### Introduction

The Advanced Peripheral Bus (APB) is part of the Advanced Microprocessor Bus Architecture (AMBA) protocol family. This protocol is a single master multi slave and set guidelines for transactions between the master and its low-bandwidth peripherals, the slaves. The APB protocol signal transactions are only related to the rising edge of the clock and every transaction takes at least two cycles. It can be used to provide access to the programmable control registers of peripheral devices. Furthermore, the APB is a low-cost interface that is optimal for minimal power consumption.

The figure bellow (Key to timing diagram conventions) explains the timing diagrams in the following sections. Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Figure 1: Key to timing diagram of APB protocol

The signals which are part of APB protocol are listed and described in the table below:

|  |  |  |
| --- | --- | --- |
| Signal | Source | Description |
| PCLK | Clock source | Clock. The rising edge of PCLK times all transfers on the APB. |
| PRESETn | System bus equivalent | Reset. The APB reset signal is active LOW. This signal is normally connected  directly to the system bus reset signal. |
| PADDR | Master | Address. This is the APB address bus. It can be up to 32 bits wide and is driven  by the peripheral bus bridge unit. |
| PSELx | Master | Select. The APB bridge unit generates this signal to each peripheral bus slave.  It indicates that the slave device is selected and that a data transfer is required.  There is a PSELx signal for each slave. |
| PENABLE | Master | Enable. This signal indicates the second and subsequent cycles of an APB  transfer. |
| PWRITE | Master | Direction. This signal indicates an APB write access when HIGH and an APB  read access when LOW. |
| PWDATA | Master | Write data. This bus is driven by the peripheral bus bridge unit during write  cycles when PWRITE is HIGH. This bus can be up to 32 bits wide. |
| PREADY | Slave | Ready. The slave uses this signal to extend an APB transfer. |
| PRDATA | Slave | Read Data. The selected slave drives this bus during read cycles when  PWRITE is LOW. This bus can be up to 32-bits wide. |
| PSLVERR | Slave | This signal indicates a transfer failure. APB peripherals are not required to  support the PSLVERR pin. This is true for both existing and new APB  peripheral designs. Where a peripheral does not include this pin then the  appropriate input to the APB bridge is tied LOW. |

Table 1: APB signal description

The PADDR,PWRITE,PWDATA signals are common among all the slaves, however there are as many PSEL signals as slaves, and for each slave one PRDATA from it to the master. The following shows the block diagram between master and slave of APB:



Figure 2: APB block diagram

#### Operating states

The figure bellow describes the operating states of the protocol:



Figure 3: APB operating states

The state machine operates through the following states:

**IDLE** - This is the default state of the APB.

**SETUP** - When a transfer is required the bus moves into the SETUP state, where the appropriate select signal, PSELx, is asserted. The bus only remains in the SETUP state for one clock cycle and always moves to the ACCESS state on the next rising edge of the clock.

**ACCESS** - The enable signal, PENABLE, is asserted in the ACCESS state. The

address, write, select, and write data signals must remain stable during

the transition from the SETUP to ACCESS state. Exit from the ACCESS state is controlled by the PREADY signal from the slave:

• If PREADY is held LOW by the slave then the peripheral bus remains in the ACCESS state.

• If PREADY is driven HIGH by the slave then the ACCESS state is exited and the bus returns to the IDLE state if no more transfers are required. Alternatively, the bus moves directly to the SETUP state if another transfer follows.

### Transfers

Each transfer consists of two cycles: one for the SETUP state and another for the ACCESS state. There are three types of transfers: write transfers, read transfers and error response transfers. In addition, write and read transfers can be with or without wait states, that are SETUP states which follow an ACCESS state instead of going to IDLE STATE.

#### Write Transfers

##### Write Transfers without wait states

A write transfer without wait states consist of two clock cycles: in the first (the SETUP STATE) the signals: address (PADDR), write data (PWDATA), write (PWRITE) and select (PSEL) are asserted. PADDR is asserted to the desired address where the data is supposed to be written, PWDATA is asserted to the desired data to be written, PWRITE is asserted HIGH and PSEL is asserted HIGH only for the specific slave which the write command is for, the rest of the PSEL lines are driven LOW. These signals remain unchanged through the second cycle.

In the second cycle (the ACCESS state) the slave sets the enable signal (PENABLE) HIGH. The ready signal (PREADY) is set HIGH by the slave in order the informed the master that the slave is ready to receive the data, which is latched by the slave in the rising edge ending the second clock cycle. After this last clock rising edge, PREADY is driven LOW by the slave, PENABLE is driven LOW by the master, and PSEL is driven LOW by the master (unless the transfer is to be followed immediately by another transfer to the same slave, in which case the signals PENABLE and PSEL remain as they are) meaning that the transfer is over.

In Figure 4 an example of write transaction with no wait states can be seen, with the first cycle of the transfer being from T1 to T2 and the second cycle from T2 to T3.



Figure 4: APB write transfer with no waits

##### Write Transfers with wait states

The first cycle of the transfers is the as the transfers without wait states. During the ACCESS state, when PENABLE is HIGH, the transfer can be extended by driving the PREADY LOW. The signals PADDR, PWRITE, PSEL, PENABLE and PDATA remain unchanged from the end of the first cycle (SETUP state) until the data is latched by the slave, which occurs at the first rising clock edge after the slave sets the PREADY signal HIGH. After this clock rising edge, PREADY is driven LOW by the slave, PENABLE is driven LOW by the master, and PSEL is driven LOW by the master meaning that the transfer is over (unless the transfer is to be followed immediately by another transfer to the same slave, in which case the signals PENABLE and PSEL remain as they are) .

In Figure 5 an example of write transaction with wait states can be seen, with the first cycle of the transfer being from T1 to T2,two wait states occur from T2 until T4 and the last cycle of the transfer from T4 to T5 , in which the slave sets the PREADY signal HIGH and at the end of this cycle the data is latched by the slave.



Figure 5: APB write transfer with wait states.

#### Read Transfers

##### Read Transfers without wait states

A read transfer without wait states consist of two clock cycles: in the first (the SETUP STATE) the signals: address (PADDR), write (PWRITE) and select (PSEL) are asserted. PADDR is asserted to the desired address where the data is supposed to be read, PWRITE is asserted LOW and PSEL is asserted HIGH only for the specific slave which the write command is for, the rest of the PSEL lines are driven LOW. These signals remain unchanged through the second cycle.

In the second cycle (the ACCESS state) the slave sets the enable signal (PENABLE) HIGH. The PRDATA signal is set by the slave according to the data in stored in the desired address(the address which is set in PADDR signal) and the ready signal (PREADY) is set HIGH by the slave in order the informed the master that the slave is ready to send the data. The data in PRDATA signal is latched by the master in the rising edge ending the second clock cycle. After this last clock rising edge, PREADY is driven LOW by the slave, PENABLE is driven LOW by the master, and PSEL is driven LOW by the master (unless the transfer is to be followed immediately by another transfer to the same slave, in which case the signals PENABLE and PSEL remain as they are) meaning that the transfer is over.

In Figure 6 an example of write transaction with no wait states can be seen, with the first cycle of the transfer being from T1 to T2 and the second cycle from T2 to T3.



Figure 6: APB read transfers with no wait states

##### Read Transfers with wait states

The first cycle of the transfers is the as the first cycle of transfer without wait states. During the ACCESS state, when PENABLE is HIGH, the transfer can be extended by driving the PREADY LOW. The signals PADDR, PWRITE, PSEL and PENABLE remain unchanged from the end of the first cycle (SETUP state) until the data is latched by the master, which occurs at the first rising clock edge after the slave sets the PREADY signal HIGH. After this clock rising edge, PREADY is driven LOW by the slave, PENABLE is driven LOW by the master, and PSEL is driven LOW by the master meaning that the transfer is over (unless the transfer is to be followed immediately by another transfer to the same slave, in which case the signals PENABLE and PSEL remain as they are) .

In Figure 7 an example of read transaction with wait states can be seen, with the first cycle of the transfer being from T1 to T2,two wait states occur from T2 until T4 and the last cycle of the transfer from T4 to T5 , in which the slave sets the PREADY signal HIGH and at the end of this cycle the data is latched by the master.



Figure 7:APB read transfer with wait states.

#### Error response

Some APB peripheral offer a way of indicating that an error occurred during a transfer with the PSLVERR signal. Errors can occur both in read and write transfers, and the signal PSLVERR is only considered valid during the last cycle of an APB transfer, when PSEL, PENABLE, and PREADY are all HIGH.

It is recommended, but not mandatory, that you drive PSLVERR LOW when it is not

being sampled. That is, when any of PSEL, PENABLE, or PREADY are LOW.

Transactions that receive an error, might or might not have changed the state of the

slave. This is peripheral-specific, and either is acceptable.

When a write transaction receives an error, this does not mean that the register within the slave has not been updated. Read transactions that receive an error can return invalid data.

There is no requirement for the slave to drive the data bus to all 0s for a read error.

APB slaves are not required to support the PSLVERR pin. This is true for both

existing and new APB peripheral designs. Where a slave does not include this pin

then the appropriate input to the master is tied LOW.

##### Error response in a write transfer

When there is an error in a write transfer and the slave in the transfer has an active PSLVERR signal, during the last cycle of the transfer (when PSEL, PENABLE, and PREADY are all HIGH) PSLVERR is driven HIGH, informing the master about the error in the transaction. These can be seen in Figure 8:



Figure 8: APB error in write transfer

##### Error response in a write transfer

When there is an error in a read transfer and the slave in the transfer has an active PSLVERR signal, during the last cycle of the transfer (when PSEL, PENABLE, and PREADY are all HIGH) PSLVERR is driven HIGH, informing the master about the error in the transaction. These can be seen in Figure 9:



Figure 9 : APB read in write transfer

## Paper summary

This section is a summary of the paper which is the base for this project, “*FPGA Implementation of K-means Algorithm for Bioinformatics Application: An Accelerated Approach to Clustering Microarray Data*” by Hanaa M. Hussain, Khaled Benkrid, Huseyin Seker, Ahmet T. Erdogan.

The motivation of the paper is the acceleration of the K means algorithm in order to process Microarrays which is a technique used in genome experiments to measure expression level of many thousands of genes simultaneously.

### K means clustering distance computation

According to the paper, distance computation is the most computationally demanding part, and where most of the K-means processing time occurs. Therefore, one aspect for improving the implementation of the algorithm is by accelerating the distance computation.

One of the widely used distance metrics incorporated with K-means clustering is the Euclidean metric and it is easy to implement. The Euclidean distance metric from point *x* to centroid (both with “n” dimensions) in iteration “*t*” is given by:

However, it also consumes a lot of computational resources when implemented in hardware due to the multiplication operation used for obtaining the square operation.

Thus, the paper presents an alternative distance metric called the Manhattan distance to be used for the classification step of the algorithm. The Manhattan metric from point *x* to centroid (both with “n” dimensions) in iteration “*t*” is given by:

The Manhattan metric according to the paper performed faster than the Euclidean metric, because it does not require calculating the square, offering better exploitation of parallelism and speed twice than that obtained by Euclidean distance. However, the accuracy of this distance measure was found to be slightly inferior to the Euclidean metric, but results were still within an acceptable error.

### K means past implementations and improvements

The paper shows few different implementation methods and their advantages/disadvantages regarding different aspect of performance, elaborate later.

* Implementing a hardware unit on FPGA board which calculate parallelly the distance(by using Manhattan metric) of each point from the input data to all cluster’s centroids. The input data was stored in a host, brought to the computational unit for the distance calculation and the result were sent back to the host for new means calculations.

Advantages:

This implementation allowed the input data to be at any size since the storage of the data was a responsibility of the host. Moreover, this implementation achieved a speed-up of 15x.

Disadvantages:

The communication overhead between the host and the FPGA board.

* Storing the data in a SRAM memory unit used exclusively for the distance calculation unit. Familiar to the previous implementation, the distance calculation is done in hardware by three-FPGA’s, and using Manhattan metric for distance calculation.

Advantages:

Speedup of 50x of more than the 500MHz Pentium III host processor, in part because the data retrieving from the host is done only one time during the algorithm, only in the beginning.

Truncating of bit width of input data helped the design to be faster.

Disadvantages:

The paper does not suggest disadvantages, but there is a clear limit of the data sets size due to the memory unit storage capacity.

* Implementation of a hybrid fixed and floating point arithmetic units for the calculations required during the algorithm run in hardware.

Advantages:

Data transfer throughput increased.

Disadvantages:

Larger FPGA area needed for the design implementation.

* Fully implementing the algorithm steps in hardware(except the initialization step which is done in a host).The distance was calculated by Manhattan metric.

Advantages:

Speedup of 500x over matlab implantation including I/O overhead, using 3 clusters.

Disadvantages:

Lack of memory capability restricted the size of data processing can be done at one time.

A suggested disadvantage is the fact that it was tested only for a run of the algorithm with 3 clusters, which can be to few clusters to receive significant information about the data after running the algorithm. There is a lack of proof that this implementation is efficient for problems which need more than 3 clusters.

* Fully implementing the algorithm steps in hardware (except the initialization step which is done in a host). The distance was calculated by Euclidean metric.

Advantages:

Speed-up of 2x over software implementation even though the former was running at 12.5 times lower frequency than the latter. Better accuracy duo to the use of Euclidean metric.

* Fully implementing the algorithm steps in hardware(on FPGA board). In addition, utilizing a floating point divider to calculate the new means in hardware level. This approach required the use of an extra block to convert the fixed-point data to floating point, and then after the division was done, another floating to fixed-point converter was needed.

Advantages:

The host is free while the FPGA is running the algorithm.

Disadvantages:

No speed up was achieved.

In conclusion, all the mention implementations were done at least ten years ago, so it is to be anticipated better timing performance in the same designs duo to the fact that today’s resources outnumber those used in some of the above mentioned implementations.

### The paper’s implementation proposal

The main implementation described in the paper is implementing all algorithm steps on hardware level, using fixed-point arithmetic only. First, creating a module capable of running the algorithm with 8 clusters and then using the rest available area of the FPGA to duplicate this module as many times as possible in order the increase the parallelism.

#### Preliminary analysis for Hardware implementation

In order to set the design requirements, the paper presents some analysis. By analyzing the future data inputs determining the common data size, dynamic range, precision and memory capacity.

After the dynamic range and precision of the input data is determined, the word length needs to be decided. This is done in the paper by calculating the minimum number of bits required to represent any word which can be part of the input data. The integer part of the word should have as many bits as:

The fractional part of the world should have as many bits as:

This calculation should be done for the word length of the input data, as well as the word length of the distances and the accumulators.

Moreover, there is a need the determined the memory capacitance needed input data, centroids and results. The ideal situation would be is to have enough Block Rams to store all datasets, and avoid memory access bottleneck. However, this is not always the case especially when using huge datasets, thus streaming data from an external memory is a possible option.

#### Hardware architecture and design

The architecture and design of the algorithm implementation is as in the figure below:

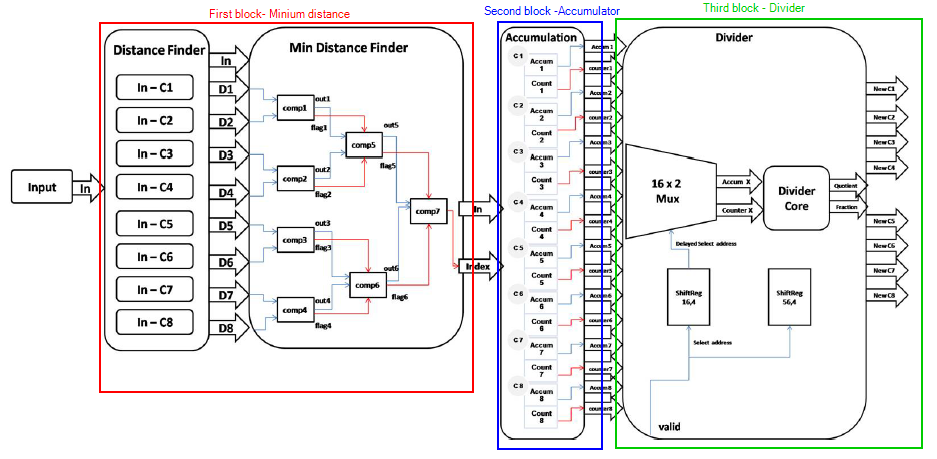


Figure 10 : The paper's implementation design divided by blocks

As it can be seen, the design is based on three blocks. The first block is used to calculate distances. The second block consists of assigning points to one of the eight clusters based on the results of the previous block. The third block is a sequential divider which calculates the new means in hardware.

##### Minimum distance finder block

The input data is stored in Block RAMs within the FPGA, and the initial centroids are stored in registers within the FPGA. The first block initially calculates distances between each data point and the cluster’s centroids. In the paper’s design eight clusters are used, therefore it has eight distance calculating processing elements working in parallel. The first block reads one data point from the on chip Block RAMs every clock cycle, obtains the eight distances simultaneously, and then obtains the absolute values of these distances. Secondly, these eight absolute distances run through a comparator tree (as shown in Figure 10 )to obtain the minimum distance for each data point and its index. This takes two clock cycles for it to complete. This whole process is fully pipelined to have a throughput of one result every clock cycle, but it has a latency of four clock cycles: one for reading the input data point and obtaining the distances, one for obtaining the absolute of these distances, two for the comparison tree to obtain the minimum distance and its index.

##### Accumulation block

The second block assigns the points to one of the eight cluster based on the results of the previous block (the point itself and the index of the cluster it should be assigned to) and counting the number of points in every cluster. The outputs of this block are eight accumulators and eight counters. This block has a throughput of one result per clock cycle with latency of one clock cycle. However, the final results will be passed to the next block when accumulators finish assigning all points to the accumulator.

##### Divider block

The third block calculates the new means in hardware. The latency of the

divider is 60 clock cycles and the throughput is one result per clock cycle. And since we are calculating eight means sequentially, the total time in which the divider will be active is 68 clock cycles. The divider itself was obtained using the core generator tool available with Xilinx ISE Design Suite 12.2. The divider block is activated by the previous block that is when the second block finishes assigning all points to clusters.

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##### Convergence

The process iterates until an end condition is reached and tested for inside the controller, which we decided to be reaching a point where previous centroids do not vary from newly calculated ones, with an acceptable 1% error.

#### Implementation results

Simulation results show that it takes 2971 clock cycles, to cluster 2905 points (415 × 7) assuming that data are already written to Block RAMs. The algorithm converged after 25 iterations, thus taking a total of 74275 clock cycles. This result does not take into consideration the time needed to write data to the FPGA Block RAMs, which is also 2905 clock cycles. However, the result does include the time to write results to the FPGA Block Rams.

In the paper a comparison between the implementation in hardware and in software was done, not considering the time needed to write data to the FPGA block RAMs . The software implementation was done with Matlab and it took an average execution time of the model for 1000 runs of the algorithm was 0.0062 ± 1.22e-4 s, with minimum execution time of 0.0060 s and maximum execution time of 0.0072 s. These results are based on initial centroids being pre defined and given as an input to the algorithm. The hardware implementation on the other hand converged after 25 iterations, thus taking a total of 74275 clock cycles. This result does not take into consideration the time needed to write data to the FPGA Block RAMs, which is also 2905 clock cycles. However, the result does include the time to write results to the FPGA Block Rams.

### Hardware Synthesis Results

The described above design was implemented on a FPGA Xilinx XC4VLX25-10SF363 using just a single core, and a maximum clock frequency of 126 MHz was achieved. This single core occupies 2.208 slices, which is only 20% of the FPGA floor area. As a result of the large available area in the FPGA after the implementation and n order to improve results the paper authors replicated the whole design five times before running out of floor area. This approach can accelerate the run time of the algorithm by five times and provide a server solution for processing multiple datasets simultaneously. In the paper, this approach was implemented using the same datasets and obtained a maximum frequency of 124 MHz, and consumed 99 % of the FPGA floor area.

For the single core design, simulation results showed that it takes about 2971 clock cycles to complete one full iteration, and the datasets required 25 iterations to converge, thus hardware execution time is just 589 μs, given that the clock frequency is 126 MHz

The implemented hardware achieved high timing performance, with speed-up of 10.3x for the case when implementing the single core, and 51.7x for the case when implementing the five cores approach.

### Paper’s conclusion

The paper in discussion presented FPGA hardware design of the K-means algorithm. Due to applying concepts of pipelining, parallelism, and multicore processing, results show that for the input data used in the paper (Microarray data) there was a speed up potential on implementing the K means algorithm on hardware level.

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